

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
22 January 2004 (22.01.2004)

PCT

(10) International Publication Number
WO 2004/008641 A1

(51) International Patent Classification⁷: **H03K 19/173**

(74) Agent: DUIJVESTIJN, Adrianus, J.; Philips Intellectual Property & Standards, Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(21) International Application Number:
PCT/IB2003/002714

(22) International Filing Date: 4 July 2003 (04.07.2003)

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02077755.3 10 July 2002 (10.07.2002) EP

(71) Applicant (*for all designated States except US*): KONIN-
KLJKE PHILIPS ELECTRONICS N.V. [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

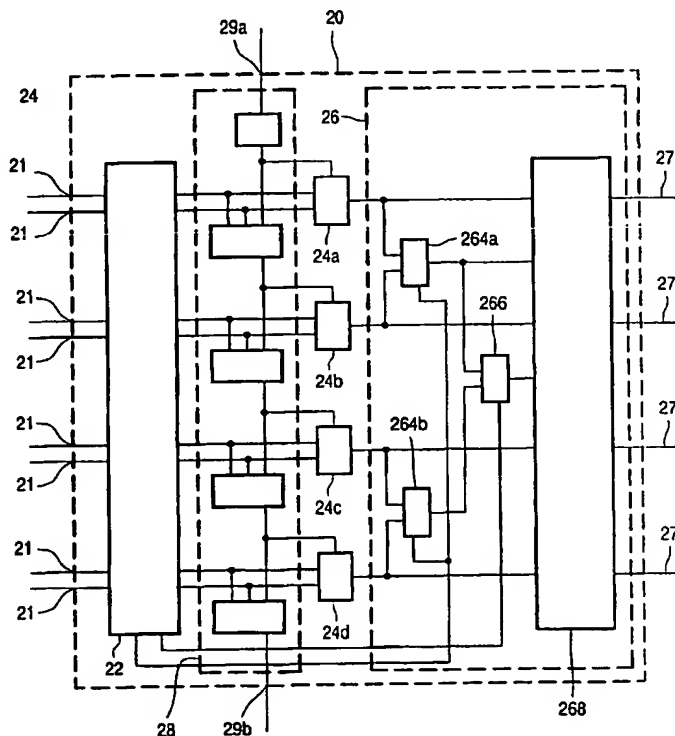
(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(72) Inventor; and

(75) Inventor/Applicant (*for US only*): LEJTEN-NOWAK,
Katarzyna [PL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA
Eindhoven (NL).

[Continued on next page]

(54) Title: ELECTRONIC CIRCUIT WITH ARRAY OF PROGRAMMABLE LOGIC CELLS



(57) Abstract: An electronic circuit has a programmable logic cell with a plurality of programmable logic units that are capable of being configured to operate in a multi-bit operand mode and a random logic mode. The programmable logic units are coupled in parallel between an input circuit and an output circuit. The input circuit can be configured to supply logic input signals from the same combination of the logic inputs to the programmable logic units in the random logic mode. In the multi-bit operand processing mode the input circuit is configured to supply logic input signals from different ones of the logic inputs to the programmable logic units. The programmable logic units are coupled to successive positions along a carry chain at least in the multi-bit operand mode, so as to process carry signals from the carry chain. The output circuit selects an output signal from the programmable logic units under control of further input signals in the random logic mode and passes outputs from the programmable logic units in parallel in the multi-bit operand mode.

WO 2004/008641 A1